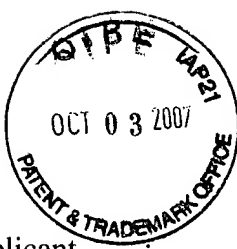


RFG.006CP1



PATENT

AF 3739  
EFW

Applicant : Robert F. Gazdzinski  
App. No. : 09/817,842  
Filed : March 26, 2001  
For : **ENDOSCOPIC SMART  
PROBE AND METHOD**  
Examiner : Leubecker, John P.  
Group Art Unit: 3739



27299

PATENT & TRADEMARK OFFICE

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

October 1, 2007  
(Date)

Robert F. Gazdzinski  
Reg. No. 39,990

**TRANSMITTAL LETTER**

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Sir:

Transmitted herewith in the above-entitled application are the following:

- (X) Appeal Brief Pursuant to 37 CFR 41.37 including Appendix I-Claims, Appendix II-Evidence, and Pre-Appeal Brief Request correspondence and Notice of Panel Decision-Appendix III (31 Pages).
- (X) A small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified statement previously submitted.
- (X) Return prepaid postcard.
- (X) The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required to Deposit Account No. 501423. A duplicate copy of this sheet is enclosed.

GAZDZINSKI & ASSOCIATES

Dated: October 1, 2007

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

5    Applicant:    Robert F. Gazdzinski                      Appl. No.:    09/817,842  
     Examiner:    Leubecker, John P.                      Gr. Art Unit:    3739  
     Filing Date:    03/26/2001  
     For:            **ENDOSCOPIC SMART PROBE AND METHOD**

10                      **APPEAL BRIEF PURSUANT TO 37 CFR 41.37**

Dear Sir or Madam:

     In reply to the *Notice of Panel Decision from Pre-Appeal Brief Review* dated March 29,  
2007, and the Final Office Action mailed October 18, 2006 ("Office Action"), Applicant herein  
15    files an appeal brief for the above-identified application:

*Real party in interest*

     Robert F. Gazdzinski (Applicant and inventor for Application Serial No. 09/817,842) is  
20    the real party in interest.

*Related appeals and interferences*

     A pre-appeal brief request for review was filed with the U.S. Patent & Trademark Office  
25    (USPTO) on February 23, 2007. A determination was received on March 29, 2007 that held that  
the application remains under appeal because there is at least one actual issue for appeal.  
Applicant has included as Appendix III (Related Proceedings) herein a copy of the pre-appeal  
brief request correspondence, and disposition by USPTO.

30    *Status of Claims*

     Claims 15-26, 34-41 and 46-55 are now pending.

     All claims stand rejected, as detailed below.

35        Claims 15, 16, 35, 36, 38-41, 46, and 50-53 are being appealed herein.

*Status of Amendments*

40        Applicant has not submitted amendments to any of the claims subsequent to final  
rejection (see Final Office Action dated October 18, 2006) of the above-identified claims.

Summary of Claimed Subject Matter

Please note that all citations to various embodiments of components for the claims below are exemplary only, and not an exhaustive list of all components described in the specification that might meet a given description.

Moreover, all citations are referenced to the specification as originally filed.

**Claim 15** - Independent Claim 15 describes a probe for autonomously operating within the intestinal tract of a living human (Fig. 1). The probe comprises at least one sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) capable of collecting information relating to the human; a data processor (Fig. 5, item 520, Fig. 12, items 1025 and/or 1024; Fig. 16a, item 1602, Fig. 17, item 520, etc.) and a communications device (Fig. 6, item labeled "data transfer"; Fig. 7, item 300; Fig. 12, item 1027; Fig. 16, item 1610; Fig. 16b (all); Fig. 17, item 1702, etc.). Claim 15 also requires that the data processor and communications device are formed on a single semi-conductive die (Fig. 16a, item 1602, claim 5 as originally filed, page 49, lines 23-30).

**Claim 35** - Independent Claim 35 describes a probe for autonomously operating within the intestinal tract of a living organism (Fig. 1). The probe is adapted for use in a multi-probe environment (page 52, line 23 through page 53, line 2 of specification), and comprises: at least one sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) capable of collecting information relating to the organism; a data processor (Fig. 5, item 520, Fig. 12, items 1025 and/or 1024; Fig. 16a, item 1602, Fig. 17, item 520, etc.) adapted to process at least a portion of said information to produce data; and a communications device (Fig. 6, item labeled "data transfer"; Fig. 7, item 300; Fig. 12, item 1027; Fig. 16, item 1610; Fig. 16b (all); Fig. 17, item 1702, etc.) adapted to transfer at least a portion of the data or said information off-probe. The communications device is further adapted to minimize interference with other communications devices operated proximate said probe in the aforementioned multi-probe environment (pages 52-53 generally; page 54, line 10).

**Claim 38** - Independent Claim 38 describes a probe for autonomously operating within the intestinal tract of a living organism, which comprises: at least one sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) capable of collecting information relating to said organism; and a data processor (Fig. 5, item 520, Fig. 12, items 1025 and/or 1024; Fig. 16a, item 1602, Fig. 17, item 520, etc.) adapted to process at least a portion of said information. Claim 38 further requires that the data processor is designed so as to specifically consider both die size and power consumption for a given processor speed through at least elimination of gates that would otherwise be present but for the design considerations (page 50, line 20 through page 51, line 15).

**Claim 39** - Independent Claim 39 describes a substantially autonomous intestinal device manufactured by the process comprising: providing a sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) for said intestinal device, said sensor being capable of generating data; generating a design for an integrated circuit useful with said device (page 50, line 20 through page 51, line 15), said design including at least one of hardware and

software extensions particularly adapted for the processing of said sensor data (page 49, line 23 through page 51, line 2); converting said design to an integrated circuit (page 51, lines 25-30); and incorporating said integrated circuit within said probe. The integrated circuit must be in operative communication with the sensor (Figs. 16a and 16b).

**Claim 40** - Independent Claim 40 describes a substantially autonomous intestinal device manufactured by the process comprising: providing a sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) for said intestinal device, said sensor being capable of generating data; providing a communications interface (Fig. 6, item labeled "data transfer"; Fig. 7, item 300; Fig. 12, item 1027; Fig. 16, item 1610; Fig. 16b (all); Fig. 17, item 1702, etc.) for transferring data; generating a design for an integrated circuit useful with said device, the design having a processor core associated therewith (Fig. 16a), and being adapted to integrate said processor core and at least a portion of the communications interface onto a single semi-conductive die (Fig. 16a, Claim 5 as originally filed, page 49, lines 23-30); fabricating said semi-conductive die having said integrated circuit (page 51, lines 25-30); and incorporating the die within the probe (Fig. 16).

**Claim 46** - Independent Claim 46 describes an autonomous intestinal probe. The probe comprises at least one image sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) and a data processor (Fig. 5, item 520, Fig. 12, items 1025 and/or 1024; Fig. 16a, item 1602, Fig. 17, item 520, etc.) operatively coupled thereto. The data processor comprises at least one instruction particularly adapted for performing mathematical operations necessary for processing of data from said at least one image sensor (page 50, lines 7-19; page 51, line 16-24).

**Claim 50** - Independent Claim 50 describes an autonomous intestinal probe having a sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.), communications interface, and a data processor (Fig. 5, item 520, Fig. 12, items 1025 and/or 1024; Fig. 16a, item 1602, Fig. 17, item 520, etc.) operatively coupled to both said sensor and said interface. The data processor comprises at least one instruction particularly adapted for performing mathematical operations necessary for processing data from the at least one image sensor for transmission over the at least one interface (page 50, lines 7-19; page 51, line 16-24).

Grounds of Rejection to be Reviewed

Claims 15-26, 34-41 and 46-55 are now pending. All claims stand rejected, as detailed below:

Claims 16, 36, 39, and 53 stand rejected under 35 USC 112(2).

Claims 35, 38-41, 46, 48, and 50-53 stand rejected under 35 USC 102(e) over Brune.

Claims 15, 16, 35, 38-41, and 53 stand rejected under 35 USC 102(b) over Alfano.

Claims 15-20, 23, 35, 40, 41 and 51-53 stand rejected under 35 USC 103(a) over Brune in view of Banyai, et al.

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Claims 21 and 22 stand rejected under 35 USC 103(a) over Brune in view of Banyai, et al and Kratz et al.

Claims 24, 25 and 34 stand rejected under 35 USC 103(a) over Brune in view of Banyai, et al and Souissi, et al.

Claim 26 stands rejected under 35 USC 103(a) over Brune in view of Banyai, et al and either Roberts, et al. or PulseON article.

Claims 36 and 37 stand rejected under 35 USC 103(a) over Brune in view of Souissi, et al

Claim 47 stands rejected under 35 USC 103(a) over Brune in view of Kratz et al.

Claim 47 stands rejected under 35 USC 103(a) over Brune in view Kratz et al.

Claims 49 and 55 stand rejected under 35 USC 103(a) over Alfano in view of Seiko Epson.

Claim 54 stands rejected under 35 USC 103(a) over Brune in view of Banyai, et al and Fette, et al.

**a. Section 112 – Applicant is appealing the finding that:**

(i) Claim 16 is indefinite under Section 112(2);

(ii) Claim 39 is indefinite under Section 112(2); and

(iii) Claim 36 is indefinite under Section 112(2).

**b. Section 102 – Applicant is appealing the finding that:**

(i) Claim 16 is anticipated under Section 102;

(ii) Claim 39 is anticipated under Section 102;

(iii) Claim 35 is anticipated under Section 102;

(iv) Claims 38-41 are anticipated under Section 102;

(v) Claim 46 is anticipated under Section 102;

(vi) Claims 50-53 are anticipated under Section 102;

(vii) Claims 15 and 40 are anticipated under Section 102; and

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(viii) Claims 39, 40, 52, and 53 should have their structural limitations given no patentable weight, and hence be anticipated under Section 102.

c. Section 103 – Applicant is appealing the finding that:

- (i) Claim 15 is obvious under Section 103;
- (ii) Claim 36 is obvious under Section 103; and
- (iii) Claim 51 is obvious under Section 103.

Arguments

**I. Section 112(2) Rejections -**

**CLEAR ERROR ON APPLICANT'S TEACHINGS AND DISCLOSURE**

**Claim 16 -**

a) Per page 2, Par. 2 of the Office Action, the Examiner rejects Claim 16 as being indefinite under Section 112(2). The Examiner asserts that Applicant's use of "extension" is vague and indefinite.

The Examiner has seemingly neglected to review the references cited by Applicant and incorporated into its specification at time of filing, including *inter alia* U.S. Patent No. 6,065,027 entitled "Data Processor with Up Pointer Walk Trie Traversal Instruction Set Extension", which clearly and unambiguously discloses: (i) extension instructions (e.g., Col. 5, line 25) ; (ii) extension hardware (e.g., ALU or "XALU") (e.g., Col. 5, line 20); (iii) extension registers (e.g., Col. 15, line 57); (iv) extension processor instruction logic circuits (e.g., Col. 5, line 15).

Moreover, as is well known by those of ordinary skill in the processor arts, the term "extensions" is a generic term that can refer to hardware, instructions, and even other types of facilities. See, e.g., the following exemplary citations from ARC (see discussion of exemplary ARC processor on page 51 of Applicant's specification as filed), a well known extensible processor producer:

- 1) [http://www.arc.com/evaluations/\\_arc\\_fpx\\_wp.pdf](http://www.arc.com/evaluations/_arc_fpx_wp.pdf)

*"Introduction*

*ARCTM FPX is a new set of licensable extensions for the ARCTM 600 and ARCTM 700 families of 32-bit processor cores. The extensions provide high performance floating point math instructions which dramatically accelerate computations where high precision is required. Hardware floating point arithmetic is often required in applications such as Global Positioning Systems (GPS), printing, imaging, flat panel displays (FPD), 3D graphics transformations, sensors and measurement, and automotive controls.*

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5        *The ARC FPX extension instructions execute on the pipeline and registers of the base processor core with only a small amount of special purpose logic. Consequently, use of ARC FPX results in minimal additional die area and little or no increase in power of the processor core."*

10        Moreover, the different types of "extensions" are typically used with one another, as in the '027 patent. For the Examiner to say that the term "extension" is unsupported or vague therefore respectfully comprises clear error.

15        **Claim 39 -**

20        Regarding Claim 39, similar logic applies (note that a "software extension" clearly refers to a software-based extension of which an extension instruction is one particular species). Applicant's disclosure clearly has support for at least one type of software extension (extension instruction), and hence is in no way vague or indefinite.

25        **Claim 36 -**

30        Per page 2, Par. 2 of the Office Action, the Examiner rejects Claim 36 as being indefinite under Section 112(2). The Examiner asserts that Applicant's use of "*substantially unique from any other code*" is indefinite.

35        The Examiner's assertions regarding "self-fulfillment" are respectfully misplaced and incorrect. In fact, spreading codes are not necessarily substantially unique, and in fact may even repeat across several different users. As a simple example, a frequency-hopping spread spectrum (FHSS) spreading code (hopping sequence) is typically generated using an algorithm which necessarily produces the same result when seeded with the same initial value. This is how the receiver can synchronize to the same sequence or code (i.e., it uses the same algorithm and the same seed). See, e.g., the well known GSM (Global System for Mobile Communications) which uses such a code. Since the population of seeds is necessarily limited, even different users will sometimes generate the same sequence, just shifted in time.

40        Accordingly, Applicant submits that the Examiner's assertion is clear error, since at least one common instance of where spreading codes are not "substantially unique" has been presented.

45        **II. Section 102 Rejections -**

**CLEAR ERROR ON CASE LAW AND INTERPRETATION OF APPLICANT'S CLAIMS**

Per page 3, Par. 3 of the Office Action ("Note"), the Examiner asserts that Applicant's Claims 16, 39, 40, 52, and 53 are "product by process" or contain process limitations that should be given no patentable weight.

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**Claim 16 -**

Applicant respectfully submits that Examiner has seemingly taken any verb present in Applicant's Claim 16 to label the entire claim as "product by process", and therefore discount the structural or non-process limitations present therein. For example, regarding Claim 16, Applicant notes that the highlighted portions presented below are purely structural in nature:

16. (Previously presented) *The probe of Claim 15, wherein said data processor comprises at least a processor core optimized for power consumption, said optimization comprising selecting a processor core configuration including at least one extension that satisfies a target core speed criterion while minimizing gate count.*

Instead, however, the Examiner completely and improperly ignores these limitations under the rubric of "they're all process-related" (paraphrasing). Neither Brune nor Alfano nor Banyai teach or suggest anything that Applicant can find regarding "power consumption optimization". Note that if one merely leaves the word "selecting" out of Claim 16, it is completely structural in nature.

Accordingly, the Examiner not only erroneously failed to address the structural limitations in Claim 16, but has also failed to provide any citation in any of his referenced art that teach or suggest such limitations. Accordingly, this comprises clear error.

Applicant further notes that even if only the limitation "*wherein said data processor comprises at least a processor core optimized for power consumption...*" is read into Claim 16 (i.e., just removing any subsequent verbage from Claim 16), Alfano still in no way teaches or suggests such limitations.

Applicant notes that it cannot find any teaching or even remote suggestion in Alfano that its processor is in any way optimized for or remotely considers power consumption in any way. The Examiner therefore does not meet his burden under Section 102; i.e., that each and every limitation be taught explicitly or by inherency. This rejection is therefore clear error on an independent basis.

**Claim 39-**

As to Claim 39, the Examiner in effect states on page 3, Par. 3 of the Office Action that the process limitations of Claim 39 provide no patentable weight. Assuming *arguendo* that the Examiner is correct (an argument Applicant does not agree with), Applicant submits that the Examiner as none-the-less failed to produce a reference which teaches, explicitly or by inherency, all of the structural (i.e., non-process) limitations of Applicant's invention of Claim 39. Specifically, Claim 39 recites:

39. *A substantially autonomous intestinal device manufactured by the process comprising:*



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*providing a sensor for said intestinal device, said sensor being capable of generating data;*

*generating a design for an integrated circuit useful with said device, said design including at least one of hardware and software extensions particularly adapted for the processing of said sensor data;*

*converting said design to an integrated circuit; and*

*incorporating said integrated circuit within said probe, said integrated circuit being in operative communication with said sensor. {emphasis added}*

Applicant has above highlighted in Claim 39 what it believes are purely structural limitations in its claim (bold). Applicant notes that the cited basis for the anticipation rejection (Brune) in no way teaches or remotely suggests at least one of hardware and software extensions particularly adapted for the processing of said sensor data as recited in Claim 39. The citation in Brune seemingly provided by the Examiner for this limitation states:

*“Controller 7 activates and receives signals from the temperature sensor 8, controls transmitter 9 which transmits data burst via antenna 10, and controls timing/power management circuit 11. Controller 7 is externally programmed by inductive programming 12. For example, the controller 7 can be inductively programmed to set an identification code, the cycle period for data bursts, a calibration factor for the temperature sensor, etc.”*

With all due respect, this cited passage (and Brune in its totality) neither remotely teaches or suggests extensions as described and claimed by Applicant (see discussion above regarding meaning of term “extensions”). It merely describes external programming, **which literally has nothing to do with extensions as defined by Applicant.**

Accordingly, Applicant respectfully submits that the Examiner rejection of Claim 39 based on anticipation by Brune is clear error, since not every limitation of Claim 39 is taught explicitly or by inherency in Brune.

#### **Claim 35 -**

Regarding Claim 35, Applicant respectfully submits that the Examiner has failed to point out where Alfano teaches or remotely suggests minimizing interference with other communication devices **of other probes** operated proximate said probe, as recited in Claim 35. See also preamble limitations regarding “multi-probe environment”, which Applicant submits are necessary to “breathe life” into the claim (i.e., the language “other communication devices” in Claim 35 is a direct reference to the antecedent recitation of “communication device”).

Hence the Examiner’s assertions comprise clear error, since no teaching is present explicitly or by inherency.

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Applicant further notes Par. 8 of the January 12, 2006 Office Action referenced by the Examiner; note that this paragraph completely fails to provide any discussion of this limitation of Claim 35 (i.e., no discussion regarding communication interference is provided by the Examiner), thereby providing a second and independent basis for error.

#### Claims 38-41

Regarding Claim 38 - 41, Applicant respectfully submits that the Examiner has failed to point out where Alfano teaches or remotely suggests a data processor is designed so as to specifically consider both die size and power consumption for a given processor speed through at least elimination of gates that would otherwise be present but for said design considerations, as recited in Claim 38.

Applicant's claim recites a processor specifically designed for the intended application (i.e., achieving a target speed while considering die size and gate count (proportional to power consumption)). Alfano merely teaches that a processor can be placed on a semiconductor. Applicant respectfully submits that this is not even *remotely* anticipatory of the aforementioned specifically designed processor of Claim 38. Hence, the Examiner's rejection respectfully comprises clear error.

#### Claim 46 -

Regarding Claim 46, Applicant respectfully submits that the Examiner has failed to point out where Alfano teaches or remotely suggests data processor comprising at least one instruction particularly adapted for performing mathematical operations necessary for processing of data from said at least one image sensor, as recited in Claim 46. The short answer is that it does not. Alfano is completely silent on any type of instructions for its processor (and even the type or design of the processor itself. No details of any kind are provided).

Hence, the Examiner's assertions and rejection respectfully comprise clear error, since no teaching is present explicitly or by inherency as required under Section 102 anticipation.

Applicant further notes Par. 8 of the January 12, 2006 Office Action referenced by the Examiner; note that this paragraph fails to provide any discussion of this limitation of Claim 46 (i.e., the Examiner merely states in effect that "a processor has instructions and mathematical operations"; no teaching that these instructions are particularly adapted for image sensor data processing as recited in Claim 46 is present in Alfano), thereby providing a second and independent basis for error.

#### Claims 50-53 -

Similar logic Applies to Claims 50-53; since independent Claim 50 recites at least one instruction particularly adapted for performing mathematical operations necessary for processing data from said at least one image sensor for transmission over said at least one interface. Hence, Claim 53 goes even further than Claim 46, **and requires that the adaptation of the instruction**

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be for purposes of transmission over said interface (e.g., a FFT butterfly, CRC, etc; see page 50 of Applicant's specification).

This is in no way taught or remotely suggested by Alfano as required under Section 102 anticipation, and hence the Examiner's rejection comprises clear error.

**Claims 39, 40, 52 and 53 –**

Per page 4, par. 7 of the January 12, 2006 Office Action, the Examiner states that Claims 39, 40, 52 and 53 are "product by process" claims and are only bound by the structure (see last part of par. 7). As previously discussed, Applicant submits that the Examiner has erroneously failed to consider the clearly structural limitations of these claims (highlighted below for convenience):

39. *A substantially autonomous intestinal device manufactured by the process comprising:*

*providing a sensor for said intestinal device, said sensor being capable of generating data;*

*generating a design for an integrated circuit useful with said device, said design including at least one of hardware and software extensions particularly adapted for the processing of said sensor data;*

*converting said design to an integrated circuit; and*

*incorporating said integrated circuit within said probe, said integrated circuit being in operative communication with said sensor. {emphasis added}*

40. *A substantially autonomous intestinal device manufactured by the process comprising:*

*providing a sensor for said intestinal device, said sensor being capable of generating data;*

*providing a communications interface for transferring data;*

*generating a design for an integrated circuit useful with said device, said design having a processor core associated therewith, said design being adapted to integrate said processor core and at least a portion of said communications interface onto a single semi-conductive die;*

*fabricating said semi-conductive die having said integrated circuit; and*

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*incorporating said die within said probe.*

52. *The probe of Claim 16, wherein said optimization of the power consumption of said **processor core** is accomplished by:*

5 *selecting a **sensor configuration** for said sensor;*

*selecting a **communications configuration** for said probe to be used by said communications device; and*

*selecting a **processor configuration** particularly adapted to reduce the cycle count used in processing instructions necessary to implement at least one of said sensor configuration and said communications configuration.*

53. *The probe of Claim 52, wherein said act of selecting a processor configuration comprises providing at least one customized extension instruction, said at least one instruction being adapted to perform at least one function associated with said sensor configuration and/or said communications configuration with a number of processor cycles less than that required by a general purpose instruction useful for the same purpose.*

Whether Claims 39, 40, 52 and 53 are “product by process” or not is immaterial; the recited product still has to have all of the structural limitations recited in these claims, irrespective of how they made it into the recited product.

Hence, Applicant respectfully submits that the Examiner has committed clear error by failing to give any patentable weight to the aforementioned claims.

## **CLEAR ERROR OF WHAT BRUNE TEACHES**

### **Claims 15 and 40 -**

The Examiner states on page 3-4 of the Office Action (relating to Claims 35, 38-41, 46, 48 and 50) that he “*still takes the position that the circuit board of Brune, which is in part semi-conductive by nature, and is die-like (flat, wafer shaped) in shape, meets the limitations of a single semi-conductive die...*”

a) **A circuit board is not a semiconductor** - Brune in no way that Applicant can find even remotely teaches or suggests a semiconductive die (i.e., a piece of a semiconductive wafer or the like), as recited in Applicant’s Claims 15 and 40.

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The Examiner respectfully has left the word “*semi*” off of the recited limitation of “*single semiconductive die*” (see page 4, line 6, Par. 7 of the January 2006 Office Action); Brune in no way teaches or suggests a single semiconductive die for the processor and communications device. Hence, Applicant respectfully submits that this comprises clear error.

Also, Applicant submits that a circuit board is not “in part, semi-conductive by nature” as asserted by the Examiner on page 4 of the October 2006 Office Action. **Is the Examiner stating that a circuit board is semi-conductive by nature because it has a semiconductor mounted on it? Applicant can see no other basis for this statement.** This is respectfully completely unsupported by the facts, and is not consistent with proper interpretation of the term “semiconductive” as used in Applicant’s specification (i.e., silicon, GaAs, etc. chip).

Accordingly, the Examiner cannot claim inherent teaching, and hence the Section 102 rejection is improper.

Furthermore, a circuit board is not a die (the term “die” being well known to those of ordinary skill in the integrated circuit arts, especially when interpreted in light of Applicant’s detailed specification, as being a single piece of semiconductive material (e.g., silicon, GaAs, SiGe, etc.). Respectfully, Brune does not even remotely teach this.

Hence, Brune cannot support a Section 102 anticipation rejection, since it fails to teach every element explicitly or by inherency. This provides yet another independent and distinct clear basis for error.

### III. Section 103 Rejections -

Per page 3, Par. 3 of the Office Action (“Note”), the Examiner asserts that Applicant’s Claims 16, 39, 40, 52, and 53 are “product by process” or contain process limitations that should be given no patentable weight. Applicant notes this since it has bearing on the Examiner’s Section 103 rejections discussed subsequently herein.

### EVIDENCE OF NON-OBVIOUSNESS NOT CONSIDERED

#### Claim 15 -

1) With respect to any obviousness rejection (see Par. 8 of the October 2006 Office Action), Brune’s teaching of a circuit board (i.e., board level) electronics teaches away from use in a human being as now recited in Claim 15, since a board of the type described by Brune simply would not fit within a human intestinal tract (especially along with the remaining components recited in Applicant’s claimed inventions) unless properly miniaturized. Brune makes no teaching or suggestion of (i) such miniaturization, or (ii) use of his invention in a human being.

Applicant therefore submits that the failure to consider or give weight to such teaching away and/or lack of the requisite suggestion under Section 103 constitutes clear error.

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**Claim 36 -**

Applicant respectfully submits that the Examiner has failed to consider that Brune teaches away from minimizing interference with other communication devices using spread spectrum techniques.

As noted by the Examiner, Brune teaches FSK and narrowband frequency (see below), which ostensibly has the consequence of mitigating interference with other devices. Brune states:

*"The boluses include means for transmitting a signal. The transmitted signal comprises a data burst which can include an identification code for individual animals as well as temperature data. ...Each bolus produces a transmission or data burst at a time or transmit interval which has a random factor. This randomness helps ensure that, when a large number of the boluses are used, for example in a large heard of cows, the likelihood of two boluses transmitting a signal or data burst simultaneously is very low." {emphasis added}*

Hence, Brune teaches mitigation of interference through narrowband frequencies and use of short, bursted communications intended to avoid collision with one another. This respectfully teaches away from spread spectrum techniques such as Direct Sequence (DSSS) and Frequency Hopping (FHSS), which by their nature have very wide frequency spectrum (hence the term "spread"), and which necessarily have collisions.

**Claim 51 -**

Claim 51 was rejected under Section 103 over Brune in view of Banyai.

Applicant noted that "[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103." In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). See MPEP 2141.02; "The court found the inventor discovered the cause of moisture transmission was through the center plug, and there was no teaching in the prior art which would suggest the necessity of selecting applicant's plug material which was more impervious to liquids than the natural rubber plug of the prior art."

Claim 51 recites (paraphrasing, and including all limitations of its parent Claim 15):

- a probe for autonomously operating within the intestinal tract of a living **human**;
- at least one sensor capable of collecting information relating to the human;
- a data processor; and
- a communications device;
- the data processor and communications device are formed on a single semi-conductive die; and
- at least the data processor comprises an integrated circuit design specifically adapted to meet at least one power consumption criterion and at least one die size criterion associated with the probe.

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Neither Brune nor Alfano in any way demonstrate an appreciation of the (source of) the problem solved by Applicant's invention of Claim 51; i.e., reduction in physical size and power consumption of the integrated circuit so that the recited apparatus can be used more effectively in a human being.

Alfano teaches nothing of reduced power consumption, or any die size criterion, as set forth in Claim 51.

Brune teaches nothing of any of the foregoing, and further in no way teaches or suggests use in a human, as set forth in Claim 51.

Hence, the Examiner's failure to consider or give weight to this non-obviousness evidence is respectfully a basis for asserting clear error.

**CLAIMS AS PENDING - APPENDIX I**

1.-14. (Cancelled)

5           15. (Previously presented)   A probe for autonomously operating within the intestinal tract of a living human, comprising:

at least one sensor capable of collecting information relating to said human;

a data processor; and

a communications device;

10           wherein said data processor and said communications device are formed on a single semi-conductive die.

16. (Previously presented)   The probe of Claim 15, wherein said data processor comprises at least a processor core optimized for power consumption, said optimization comprising selecting a processor core configuration including at least one extension that satisfies  
15 a target core speed criterion while minimizing gate count.

17. (Previously presented)   The probe of Claim 16, wherein said processor core includes at least one sleep mode.

18. (Previously presented)   The probe of Claim 17, wherein said at least one sleep mode is adapted to selectively place portions of said processor core in a state of reduced power  
20 consumption.

19. (Previously presented)   The probe of Claim 17, wherein said at least one sleep mode is entered or exited via at least one signal generated external to said probe.

20. (Previously presented)   The probe of Claim 16, wherein said processor comprises at least one instruction, said at least one instruction being adapted to perform at least one  
25 mathematical operation.

21. (Previously presented)   The probe of Claim 20, wherein said at least one mathematical operation comprises a fast-fourier transform (FFT).

22. (Previously presented)   The probe of Claim 20, wherein said at least one mathematical operation comprises a butterfly calculation.

30           23. (Previously presented)   The probe of Claim 20, wherein said at least one mathematical operation comprises a calculation in support of error correction.



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24. (Previously presented) The probe of Claim 16, wherein said communications device comprises at least a portion of a direct sequence spread spectrum (DSSS) transceiver.

25. (Previously presented) The probe of Claim 16, wherein said communications device comprises at least a portion of a frequency hopping spread spectrum (FHSS) transceiver.

5 26. (Previously presented) The probe of Claim 16, wherein said communications device comprises at least a portion of a time-modulated ultra-wide bandwidth (TM-UWB) transceiver.

27.- 33. (Cancelled)

10 34. (Previously presented) A probe for autonomously operating within the intestinal tract of a living organism, comprising:

at least one sensor capable of collecting information related to said organism;

a data processor adapted to process at least a portion of said information to produce data;

and

15 a spread spectrum communications device adapted to transfer at least a portion of said data or said information off-probe.

35. (Previously presented) A probe for autonomously operating within the intestinal tract of a living organism and adapted for use in a multi-probe environment, comprising:

at least one sensor capable of collecting information relating to said organism;

a data processor adapted to process at least a portion of said information to produce data;

20 and

a communications device adapted to transfer at least a portion of said data or said information off-probe, said communications device further being adapted to minimize interference with other communications devices operated proximate said probe.

25 36. (Previously presented) The probe of Claim 35, wherein said communications device comprises a spread-spectrum transceiver having a spreading code that is substantially unique from any other spreading code.

37. (Previously presented) The probe of Claim 35, wherein said communications device operates in the ISM band.

30 38. (Previously presented) A probe for autonomously operating within the intestinal tract of a living organism, comprising:

at least one sensor capable of collecting information relating to said organism; and

a data processor adapted to process at least a portion of said information;

wherein said data processor is designed so as to specifically consider both die size and power consumption for a given processor speed through at least elimination of gates that would otherwise be present but for said design considerations.

5           39. (Previously presented)   A substantially autonomous intestinal device manufactured by the process comprising:

          providing a sensor for said intestinal device, said sensor being capable of generating data;

          generating a design for an integrated circuit useful with said device, said design including at least one of hardware and software extensions particularly adapted for the processing of said  
10   sensor data;

          converting said design to an integrated circuit; and

          incorporating said integrated circuit within said probe, said integrated circuit being in operative communication with said sensor.

          40. (Previously presented)   A substantially autonomous intestinal device manufactured  
15   by the process comprising:

          providing a sensor for said intestinal device, said sensor being capable of generating data;

          providing a communications interface for transferring data;

          generating a design for an integrated circuit useful with said device, said design having a processor core associated therewith, said design being adapted to integrate said processor core  
20   and at least a portion of said communications interface onto a single semi-conductive die;

          fabricating said semi-conductive die having said integrated circuit; and

          incorporating said die within said probe.

          41. (Previously presented)   The intestinal device of Claim 40, wherein said act of generating further comprises optimizing the power consumption of said die by incorporating at  
25   least one extension instruction within said core.

          42. – 45. (Cancelled)

          46. (Previously presented)   An autonomous intestinal probe having at least one image sensor and a data processor operatively coupled thereto, said data processor comprising at least one instruction particularly adapted for performing mathematical operations necessary for  
30   processing of data from said at least one image sensor.

47. (Previously presented) The probe of Claim 46, wherein said at least one instruction comprises an FFT instruction.

48. (Previously presented) The probe of Claim 46, wherein said at least one instruction comprises an instruction adapted to perform error correction.

5 49. (Previously presented) The probe of Claim 46, wherein said at least one instruction comprises an instruction adapted to perform image compression.

50. (Previously presented) An autonomous intestinal probe having a sensor, communications interface, and a data processor operatively coupled to both said sensor and said interface, said data processor comprising at least one instruction particularly adapted for  
10 performing mathematical operations necessary for processing data from said at least one image sensor for transmission over said at least one interface.

51. (Previously presented) The probe of Claim 15, wherein at least said data processor comprises an integrated circuit design specifically adapted to meet at least one power consumption criterion and at least one die size criterion associated with said probe.

15 52. (Previously presented) The probe of Claim 16, wherein said optimization of the power consumption of said processor core is accomplished by:

selecting a sensor configuration for said sensor;

selecting a communications configuration for said probe to be used by said communications device; and

20 selecting a processor configuration particularly adapted to reduce the cycle count used in processing instructions necessary to implement at least one of said sensor configuration and said communications configuration.

53. (Previously presented) The probe of Claim 52, wherein said act of selecting a processor configuration comprises providing at least one customized extension instruction, said  
25 at least one instruction being adapted to perform at least one function associated with said sensor configuration and/or said communications configuration with a number of processor cycles less than that required by a general purpose instruction useful for the same purpose.

54. (Previously presented) The method of Claim 53, wherein said at least one function comprises multiply-accumulate (MAC) operations.

30 55. (Previously presented) The method of Claim 53, wherein said at least one function comprises image data compression.

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**EVIDENCE - APPENDIX II**

**NONE**

•       **Application No.**     :     **09/817,842**  
•       **Filed**               :     **March 26, 2001**  
•

**RELATED PROCEEDINGS - APPENDIX III**

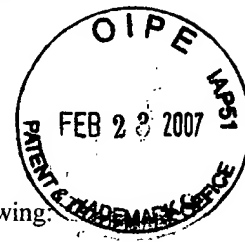
(see attachments)



Appl. No.: 09/817,842 Filing Date: March 26, 2001  
In Re: Robert F Gazdzinski Examiner: Leubecker, John P.  
Our Reference: RFG.006CP1 Group Art Unit: 3739

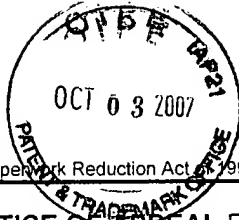
Entitled: **ENDOSCOPIC SMART PROBE AND METHOD**

Today's Date: Monday, February 19, 2007

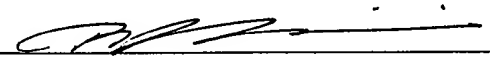



The Patent Offices' stamp hereon acknowledges receipt of the following:

Papers: Pre-Appeal Brief Request for Review (1 Page);  
Pre-Appeal Brief Request for Review Attachment (5 Pages);  
Notice of Appeal (1 Page);  
Petition for Extension of Time (1 Page);



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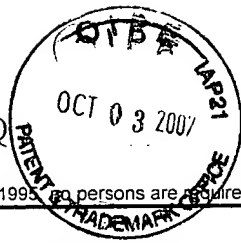
<b>NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES</b>		Docket Number (Optional)  <b>RFG.006CP1</b>
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 [37 CFR 1.8(a)] on <u>February 19, 2007</u> Signature <u></u> Typed or printed name <u>Robert F. Gazdzinski</u>		In re Application of <b>Robert F. Gazdzinski</b> Application Number <u>09/817,842</u> Filed <u>03/26/2001</u> For <b>ENDOSCOPIC SMART PROBE AND METHOD</b> Art Unit <u>3739</u> Examiner <u>Leubecker</u>
Applicant hereby appeals to the Board of Patent Appeals and Interferences from the last decision of the examiner.		
The fee for this Notice of Appeal is (37 CFR 41.20(b)(1))		\$ <u>500</u>
<input checked="" type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is:		\$ <u>250</u>
<input checked="" type="checkbox"/> A check in the amount of the fee is enclosed.		
<input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.		
<input type="checkbox"/> The Director has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.		
<input checked="" type="checkbox"/> The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. <u>501423</u> . I have enclosed a duplicate copy of this sheet.		
<input checked="" type="checkbox"/> A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.		
<b>WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</b>		
I am the		
<input type="checkbox"/> applicant/inventor.		<u></u> Signature
<input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)		<u>Robert F. Gazdzinski</u> Typed or printed name
<input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>39,990</u>		<u>858-675-1670</u> Telephone number
<input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____		<u>February 19, 2007</u> Date
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.		

<input type="checkbox"/> *Total of _____ forms are submitted.
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This collection of information is required by 37 CFR 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Doc Code: AP.PRE.REQ



PTO/SB/33 (07-05)

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**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Docket Number (Optional)

RFG.006CP1

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on February 19, 2007

Signature

Typed or printed name Robert F. Gazdzinski

Application Number

09/817,842

Filed

03/26/2001

First Named Inventor

Robert F. Gazdzinski

Art Unit

3739

Examiner

Leubecker

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐

applicant/inventor.

☐

assignee of record of the entire interest.

See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.  
(Form PTO/SB/96)

☒

attorney or agent of record.

39,990

Registration number

☐

attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34

Signature

Robert F. Gazdzinski

Typed or printed name

858-675-1670

Telephone number

February 19, 2007

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.  
Submit multiple forms if more than one signature is required, see below\*.

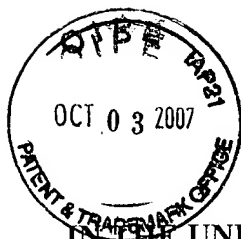
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\*Total of \_\_\_\_\_ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

5 Applicant: Robert F. Gazdzinski Appl. No.: 09/817,842  
 Examiner: Leubecker, John P. Gr. Art Unit: 3739  
 Filing Date: 03/26/2001  
 For: **ENDOSCOPIC SMART PROBE AND METHOD**

10 **PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Dear Sir:

In reply to the Office Action dated October 19, 2006 ("Office Action"), Applicant herein requests a pre-appeal brief review of the above-identified application as follows:

15 **I. CLEAR ERROR ON APPLICANT'S TEACHINGS AND DISCLOSURE**

a) Per page 2, Par. 2 of the Office Action, the Examiner rejects Claim 16 as being indefinite under Section 112(2). The Examiner asserts that Applicant's use of "extension" is vague and indefinite.

20 The Examiner has seemingly neglected to review the references cited by Applicant and incorporated into its specification at time of filing, including *inter alia* U.S. Patent No. 6,065,027 entitled "Data Processor with Up Pointer Walk Trie Traversal Instruction Set Extension", which clearly and unambiguously discloses: (i) extension instructions (e.g., Col. 5, line 25) ; (ii) extension hardware (e.g., ALU or "XALU") (e.g., Col. 5, line 20); (iii) extension registers (e.g., Col. 15, line 57); (iv) extension processor instruction logic circuits (e.g., Col. 5, line 15). As is well known by those of ordinary skill in the art, the term "extensions" is a generic term that can refer to hardware, instructions, and even other types of facilities. Moreover, the different types of "extensions" are typically used with one another, as in the '027 patent. For the Examiner to say  
 25 **that the term "extension" is unsupported or vague is therefore respectfully disingenuous, and comprises clear error.**

30 Regarding Claim 39, similar logic applies (note that a "software extension" clearly refers to a software-based extension of which an extension instruction is one particular species").  
 35 Applicant's disclosure clearly has support for at least one type of software extension (extension instruction), and hence is in no way vague or indefinite.

a) Per page 2, Par. 2 of the Office Action, the Examiner rejects Claim 36 as being indefinite under Section 112(2). The Examiner asserts that Applicant's use of "*substantially unique from any other code*" is indefinite.  
 40

The Examiner's assertions regarding "self-fulfillment" are respectfully misplaced and incorrect. In fact, spreading codes are not necessarily substantially unique, and in fact may even repeat across several different users. As a simple example, a frequency-hopping spread spectrum (FHSS) spreading code (hopping sequence) is typically generated using an algorithm which  
 45 necessarily produces the same result when seeded with the same initial value. This is how the receiver can synchronize to the same sequence or code (i.e., it uses the same algorithm and the same seed). See, e.g., the well known GSM (Global System for Mobile Communications) which

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uses such a code. Since the population of seeds is necessarily limited, even different users will sometimes generate the same sequence, just shifted in time.

Accordingly, Applicant submits that the Examiner's assertion is clear error, since at least one common instance of where spreading codes are not "substantially unique" has been presented.

## II. CLEAR ERROR ON CASE LAW AND INTERPRETATION OF APPLICANT'S CLAIMS

Per page 3, Par. 3 of the Office Action ("Note"), the Examiner asserts that Applicant's claims 16, 39, 40, 52, and 53 are "product by process" or contain process limitations that should be given no patentable weight.

Applicant notes that Examiner has seemingly taken any verb present in Applicant's claim 16 to label the entire claim as "product by process", and therefore discount the structural or non-process limitations present therein. For example, regarding Claim 16, Applicant notes that the highlighted portions presented below are purely structural in nature:

*16. (Previously presented) The probe of Claim 15, wherein said data processor comprises at least a processor core optimized for power consumption, said optimization comprising selecting a processor core configuration including at least one extension that satisfies a target core speed criterion while minimizing gate count.*

Instead, however, the Examiner completely and improperly ignores these limitations under the rubric of "they're all process-related" (paraphrasing). Neither Brune nor Alfano nor Banyai teach or suggest anything that Applicant can find regarding "power consumption optimization". Note that if one merely leaves the word "selecting" out of Claim 16, it is completely structural in nature.

Accordingly, the Examiner not only erroneously failed to address the structural limitations in Claim 16, but has also failed to provide any citation in any of his referenced art that teach or suggest such limitations. Accordingly, this comprises clear error.

## III. CLEAR ERROR OF WHAT ALFANO TEACHES

a) In furtherance of the discussion presented above under Item II., Applicant notes that even if only the limitation "*wherein said data processor comprises at least a processor core optimized for power consumption...*" is read into Claim 16 (i.e., just removing any subsequent verbiage from Claim 16), Alfano still in no way teaches or suggests such limitations. Applicant notes that it cannot find any teaching or even remote suggestion in Alfano that its processor is in any way optimized for or remotely considers power consumption in any way. The Examiner therefore does not meet his burden under Section 102; i.e., that each and every limitation be taught explicitly or by inherency. This rejection is therefore clear error.

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Filed : March 26, 2001

b) Regarding Claim 35, Applicant requests the Examiner to point out where Alfano teaches or remotely suggests minimizing interference with other communication devices operated proximate said probe, as recited in Claim 35. The short answer is that it does not, and hence the Examiner's assertions are improper and comprise clear error since no teaching is present explicitly or by inherency.

Applicant further notes Par. 8 of the January 12, 2006 Office Action referenced by the Examiner; **note that this paragraph completely glosses over this limitation of Claim 35 (i.e., no discussion regarding communication interference is even attempted by the Examiner).**

c) Regarding Claim 38 - 41, Applicant requests the Examiner to point out where Alfano teaches or remotely suggests a data processor is designed so as to specifically consider both die size and power consumption for a given processor speed through at least elimination of gates that would otherwise be present but for said design considerations, as recited in Claim 38. Applicant's claim recites a processor specifically designed for the intended application (i.e., achieving a target speed while considering die size and gate count (proportional to power consumption)). Alfano merely teaches that a processor can be placed on a semiconductor. How is this even remotely anticipatory of the aforementioned specifically designed processor?

Again, it is not, and hence the Examiner's rejection comprises clear error.

d) Regarding Claim 46, Applicant requests the Examiner to point out where Alfano teaches or remotely suggests data processor comprising at least one instruction particularly adapted for performing mathematical operations necessary for processing of data from said at least one image sensor, as recited in Claim 46. The short answer is that it does not; Alfano is completely silent on any type of instructions for its processor (and even the type or design of the processor itself. No details of any kind are provided). Hence, the Examiner's assertions are improper and comprise clear error since no teaching is present explicitly or by inherency.

Applicant further notes Par. 8 of the January 12, 2006 Office Action referenced by the Examiner; **note that this paragraph completely glosses over this limitation of Claim 46 (i.e., the Examiner merely states in effect that "a processor has instructions and mathematical operations"; no attempt to state that these instructions are particularly adapted for image sensor data processing as recited in Claim 46 is made).**

Similar logic Applies to Claims 50-53; however, this is an even more egregious case, since independent Claim 50 recites at least one instruction particularly adapted for performing mathematical operations necessary for processing data from said at least one image sensor for transmission over said at least one interface. Hence, Claim 53 goes even further than Claim 46, **and requires that the adaptation of the instruction be for purposes of transmission over said interface** (e.g., a FFT butterfly, CRC, etc; see page 50 of Applicant's specification). This is in no way taught or remotely suggested by Alfano.

#### IV. CLEAR ERROR OF WHAT BRUNE TEACHES

The Examiner states on page 3-4 of the Office Action (relating to Claims 35, 38-41, 46, 48 and 50) that he *"still takes the position that the circuit board of Brune, which is in part semi-conductive by nature, and is die-like (flat, wafer shaped) in shape, meets the limitations of a single semi-conductive die..."*

a) **A circuit board is not a semiconductor** - Brune in no way that Applicant can find even remotely teaches or suggests a semiconductive die (i.e., a piece of a semiconductive wafer or the like), as recited in Applicant's Claims 15 and 40. Applicant traverses this rejection in its entirety, and submits that it is clear error.

The Examiner respectfully has conveniently left the word *"semi"* off of the recited limitation of "single semiconductive die" (see page 4, line 6, Par. 7 of the January 2006 Office Action); Brune in no way teaches or suggests a single semiconductive die for the processor and communications device.

Also, how is a circuit board "in part, semi-conductive by nature" as asserted by the Examiner on page 4 of the October 2006 Office Action? **Is the Examiner stating that a circuit board is semi-conductive by nature because it has a semiconductor mounted on it? This is respectfully ludicrous.** The Examiner cannot claim inherent teaching, and hence the Section 102 rejection is improper.

Furthermore, a circuit board is not a die (the term "die" being well known to those of ordinary skill in the integrated circuit arts, especially when interpreted in light of Applicant's detailed specification, as being a single piece of semiconductive material (e.g., silicon, GaAs, SiGe, etc.). Where does Brune even remotely teach this? **It does not, and hence Brune cannot support an anticipation rejection, since it fails to teach every element explicitly or by inherency.**

b) **Evidence of Non-obviousness Ignored** - Moreover, with respect to any obviousness rejection (see Par. 8 of the October 2006 Office Action), Brune's teaching of a circuit board (i.e., board level) electronics teaches away from use in a human being as now recited in Claim 15, since a board as described by Brune simply would not fit within a human intestinal tract (especially along with the remaining components recited in Applicant's claimed inventions) unless properly miniaturized. Brune makes no teaching or suggestion of (i) such miniaturization, or (ii) use of his invention in a human being.

Similarly, Applicant also notes that "[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103." In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). See MPEP 2141.02; "The court found the inventor discovered the cause of moisture transmission was through the center plug, and there was no teaching in the prior art which would suggest the necessity of selecting applicant's plug material which was more impervious to liquids than the natural rubber plug of the prior art." **Brune**

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does not in any way demonstrate an appreciation of the problem solved by Applicant's claimed invention; i.e., reduction in physical size and power consumption so that the recited apparatus can be used in a human being.

5 Hence, the Examiner's failure to consider this teaching away and non-obviousness evidence is a second, distinct basis for clear error.

#### V. CLEAR ERROR – “HOUSE OF CARDS”

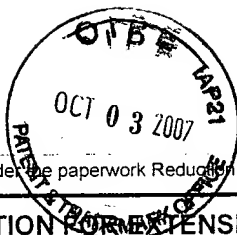
10 Applicant lastly notes and traverses the Examiner's rejections of claims which depend directly or indirectly on any of the claims previously discussed herein. Based on the foregoing, each of the bases of rejection for the previously discussed claims is clearly erroneous, and hence the Examiner's rejections of further depending claims are, respectfully, necessarily built on a house of cards. Specifically, not each and every element of each of these dependent claims is taught or suggested by the references cited by the Examiner.

15 As one specific example, consider the fact that **neither Brune nor Alfano nor Banyai nor Kratz nor Soussi nor Roberts teach or suggest anything that Applicant can find regarding “power consumption optimization”.** Hence, Claims 17, 18, 19, 20, 21, 22, 23, 24, 25, and 26, which all depend directly or indirectly from Claim 16, are necessarily not anticipated or obvious based on the art cited by the Examiner.

#### Summary

25 Applicant has herein respectfully provided at least one bases, and in many cases two or more bases, for overturning the Examiner's Section 112, 102 and/or 103 rejections of numerous now pending claims based on clear error. Accordingly, Applicant requests that these claims be allowed at the earliest opportunity.

30



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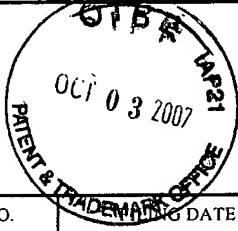
<b>PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)</b> <b>FY 2006</b> <i>(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)</i>		Docket Number (Optional) <b>RFG.006CP1</b>																									
Application Number <b>09/817,842</b>		Filed <b>03/26/2001</b>																									
For <b>ENDOSCOPIC SMART PROBE AND METHOD</b>																											
Art Unit <b>3739</b>		Examiner <b>Leubecker</b>																									
<p>This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.</p> <p>The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):</p> <table><thead><tr><th></th><th><u>Fee</u></th><th><u>Small Entity Fee</u></th><th></th></tr></thead><tbody><tr><td><input checked="" type="checkbox"/> One month (37 CFR 1.17(a)(1))</td><td>\$120</td><td>\$60</td><td>\$ <u>60</u></td></tr><tr><td><input type="checkbox"/> Two months (37 CFR 1.17(a)(2))</td><td>\$450</td><td>\$225</td><td>\$ _____</td></tr><tr><td><input type="checkbox"/> Three months (37 CFR 1.17(a)(3))</td><td>\$1020</td><td>\$510</td><td>\$ _____</td></tr><tr><td><input type="checkbox"/> Four months (37 CFR 1.17(a)(4))</td><td>\$1590</td><td>\$795</td><td>\$ _____</td></tr><tr><td><input type="checkbox"/> Five months (37 CFR 1.17(a)(5))</td><td>\$2160</td><td>\$1080</td><td>\$ _____</td></tr></tbody></table> <p><input checked="" type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27.</p> <p><input checked="" type="checkbox"/> A check in the amount of the fee is enclosed.</p> <p><input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.</p> <p><input type="checkbox"/> The Director has already been authorized to charge fees in this application to a Deposit Account.</p> <p><input checked="" type="checkbox"/> The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number <u>501423</u>. I have enclosed a duplicate copy of this sheet.</p> <p><b>WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</b></p> <p>I am the <input type="checkbox"/> applicant/inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).</p> <p><input checked="" type="checkbox"/> attorney or agent of record. Registration Number <u>39,990</u></p> <p><input type="checkbox"/> attorney or agent under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____</p> <p>_____ Signature</p> <p><u>2-19-2007</u> Date</p> <p><u>Robert F. Gazdzinski</u> Typed or printed name</p> <p><u>858-675-1670</u> Telephone Number</p> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.</p> <p><input type="checkbox"/> Total of _____ forms are submitted.</p>					<u>Fee</u>	<u>Small Entity Fee</u>		<input checked="" type="checkbox"/> One month (37 CFR 1.17(a)(1))	\$120	\$60	\$ <u>60</u>	<input type="checkbox"/> Two months (37 CFR 1.17(a)(2))	\$450	\$225	\$ _____	<input type="checkbox"/> Three months (37 CFR 1.17(a)(3))	\$1020	\$510	\$ _____	<input type="checkbox"/> Four months (37 CFR 1.17(a)(4))	\$1590	\$795	\$ _____	<input type="checkbox"/> Five months (37 CFR 1.17(a)(5))	\$2160	\$1080	\$ _____
	<u>Fee</u>	<u>Small Entity Fee</u>																									
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This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILED DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,842	03/26/2001	Robert F. Gazdzinski	RFG.006CP1	9452

27299 7590 03/29/2007  
GAZDZINSKI & ASSOCIATES  
11440 WEST BERNARDO COURT, SUITE 375  
SAN DIEGO, CA 92127

EXAMINER
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LEUBECKER, JOHN P

ART UNIT	PAPER NUMBER
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3739

MAIL DATE	DELIVERY MODE
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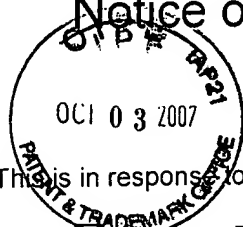
03/29/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Application Number</b> 	<b>Application/Control No.</b> 09/817,842	<b>Applicant(s)/Patent under Reexamination</b> GAZDZINSKI, ROBERT F.	
	Thomas C. Barrett	<b>Art Unit</b> 3738	
<b>Document Code - AP.PRE.DEC</b>			

## Notice of Panel Decision from Pre-Appeal Brief Review



This is in response to the Pre-Appeal Brief Request for Review filed February 23 2007.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

- ☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
- ☐ The request does not include reasons why a review is appropriate.
- ☐ A proposed amendment is included with the Pre-Appeal Brief request.
- ☐ Other:

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☒ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☒ The panel has determined the status of the claim(s) is as follows:  
 Claim(s) allowed: \_\_\_\_\_  
 Claim(s) objected to: \_\_\_\_\_  
 Claim(s) rejected: 15-26, 34-41, 46-55  
 Claim(s) withdrawn from consideration: \_\_\_\_\_

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☐ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) Thomas C. Barrett

(3) Linda Dvorak

(2) John Leubecker

(4) \_\_\_\_\_